I claim:

1. A method of generating a digital display signal from an analog signal that is limited to 2^N discrete analog levels and from a synchronization signal that defines spatial order for said digital display signal, the method comprising the steps of:

in response to a sample clock, sampling said analog signal to provide analog samples;

quantizing said analog samples to provide an M-bit digital display signal wherein M exceeds N; and

adjusting at least one of the frequency and phase of said sample clock to substantially restrict the codes of said M-bit digital display signal to 2^N different codes.

2. The method of claim 1, further including the step of generating said sample clock in response to said synchronization signal.

3. The method of claim 1, wherein said adjusting step includes the step of:

identifying spurious codes that exceed said 2^N discrete analog levels; and

adjusting at least one of said frequency and said phase to substantially eliminate said spurious codes.

4. The method of claim 1, further including the steps of:

dividing a reference signal by a divisor to form a feedback signal;

comparing said feedback signal to said synchronization signal to thereby phase lock said reference signal to said synchronization signal; and

delaying said reference signal by a delay to form said sample clock,

and wherein said adjusting step includes the steps of:

changing said divisor to thereby adjust said frequency, and

selecting said delay to thereby adjust said phase.

5. The method of claim 1, wherein M exceeds N by at least two.

6. An analog interface which genererates a digital display signal from an analog signal that is limited to 2^N discrete analog levels and from a synchronization signal that defines spatial order for said digital display signal, the interface comprising:

a phase-locked loop that includes a frequency divider and phase locks a reference signal to said synchronization signal via said frequency divider;

a clock synthesizer that introduces a phase shift to thereby generate a sample clock from said reference signal;

an analog-to-digital converter that includes:

a) a sampler that extracts analog samples from said analog signal in response to said sample clock; and

b) at least one converter stage that quantizes said analog samples into an M-bit digital display signal wherein M exceeds N; and

a clock controller that monitors said digital display signal and adjusts at least one of the divisor of said frequency divider and the delay of said clock synthesizer to substantially restrict the codes of said M-bit digital display signal to 2^N different codes.

7. The interface of claim 6, wherein said phase-locked loop includes:

a voltage-controlled oscillator that generates said reference signal; and

a phase detector that controls said oscillator in response to phase differences between said synchronization signal and a divided signal provided by said frequency divider in response to said reference signal.

8. The interface of claim 6, wherein said clock synthesizer is a delay-locked loop.

9. The interface of claim 6, wherein said clock controller includes a memory which stores said codes.

10. An interface system for converting digital data into a digital display signal, comprising:

at least one digital-to-analog converter which converts said data to an analog signal that is limited to 2^N discrete analog levels;

a signal generator that provides a synchronization signal that defines spatial order in said analog signal;

a phase-locked loop that includes a frequency divider and phase locks a reference signal to said synchronization signal via said frequency divider;

a clock synthesizer that introduces a phase shift to thereby generate a sample clock from said reference signal;

at least one analog-to-digital converter that includes:

a) a sampler that extracts analog samples from said analog signal in response to said sample clock; and

b) at least one converter stage that quantizes said analog samples into an M-bit digital display signal wherein M exceeds N; and

a clock controller that monitors said digital display signal and adjusts at least one of the divisor of said frequency divider and the delay of said clock synthesizer to substantially restrict the codes of said M-bit digital display signal to 2^N different codes.

11. The system of claim 10, wherein said phase-locked loop includes:

a voltage-controlled oscillator that generates said reference signal; and

a phase detector that controls said oscillator in response to phase differences between said synchronization signal and a divided signal provided by said frequency divider in response to said reference signal.

12. The system of claim 10, wherein said clock synthesizer is a delay-locked loop.

13. The system of claim 10, wherein said clock controller includes

a memory which stores said codes.